Amendment to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): A data processing device, which decodes and executes instructions of a predetermined length instruction set containing a spare field, comprising:

an instruction cache memory;

a predecode-processor which decodes operation codes contained in first fields of each of said instructions to generate a piece of information, said information representing whether said instruction is a branch instruction or not, and sets ~~transfers~~ the information in ~~as~~ said spare field of each of said instructions~~,; and~~

wherein the instruction cache memory holds the information in said spare field of each of said instructions;

an instruction flow unit which controls an executing sequence of said instructions based on information of said spare field, when executing instructions loaded from said cache memory,

wherein the instruction flow unit issues commands to fetch an instruction of a branch destination, when it determines that said instruction is a branch instruction according to said information of the said spare field, and

wherein the spare field is a reserved field or an open field in the instructions of said predetermined length instruction set.

2. – 7. (canceled).

8. (previously presented): The data processing device according to claim 1,:

wherein the instruction flow unit comprises:

a queuing buffer temporarily storing instructions loaded from said instruction cache memory; and

a target buffer which holds an address of said branch destination, said instruction of said branch destination, and a following address of said address of said branch destination,

wherein said instruction flow unit divides one branch operation into a prepare target instruction and a branch procedure instruction,

wherein said prepare target instruction commands calculating of said address of said branch destination and fetching of said instruction of said branch destination,

wherein said branch procedure instruction commands branch condition checks and branch procedures.

9. (previously presented): The data processing device according to claim 8,

wherein said instruction flow unit issues commands to load said instruction of said branch destination and said following address from said target buffer when said instruction flow unit determines that said instruction is a branch procedure instruction according to said information of said queuing buffer.

10. – 20. (canceled)